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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,433	09/16/2003	Wen-Ching Chen	MR1683-703	9840

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ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
WILLIAMS, DON J	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/662,433	CHEN, WEN-CHING	
	Examiner	Art Unit	
	Don Williams	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 16, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Glenn et al (6,342,406).

As to claim 5 Glenn et al disclose a chip scale package (100) having multiple bumps (112A, 112B) formed on a top face of the semiconductor image sense chip (102) and a transparent layer (140A) attached to the top face of the semiconductor image sense chip (102), and the transparent layer (140A) having a thickness being equal to each of the bumps (112A, 112B), (see figure 3, column 8, lines 1-11).

As to claim 6, Glenn et al disclose a chip scale package (100) with a transparent layer (140A) is a transparent glass plate including multiple penetration holes (118C, 118D), each penetration hole (118C, 118D) aligning with a corresponding one of the multiple bumps (112A, 112B) wherein each bump (112A, 112B) extends to a top face of the transparent glass plate (140A), (see figure 3, column 8, lines 1-11).

As to claim 7, Glenn et al disclose a chip scale package (100) with a transparent layer (140A) being a transparent glass plate having an area equal to that of the semiconductor image sense chip (102), the transparent glass plate (140A) having a periphery (PR) covered by a shelter (130S) to prevent the light from laterally penetrating into the chip scale package structure (100) and influencing the quality of the images collected by the chip scale package structure (100), wherein a metal solder ball (122A, 122B) is planted on a free end of each of the multiple bumps (112A, 112B) and electrically connected to a flexible printed circuit (FPC), the FPC having a window (110) and corresponding to a sensing area (104) of the semiconductor image sense chip (102) and a conducting circuit including multiple first solder points (114) formed near a periphery (PR) of the window (110), the number of the first solder points (114) corresponding to that of the bumps (112A, 112B), the conducting circuit including multiple second solder points (116) formed near one side of the FPC, (see figure 1, column 5, lines 1-5, figure 3, column 7, lines 1-17, column 8, lines 1-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al in view of Park et al (6,211,461).

As to claim 1, Glenn et al disclose a chip scale package (100) for an image sensor (102) with a semiconductor image sense chip (102), multiple bonding pads (106A, 106B) formed on the top face of the semiconductor image sense chip (102), a conducting wire (118C, 118D) extending from each of the multiple bonding pads (106A, 106B) by wire bonding (114B, 114A), a transparent layer (140A) on the top surface of the semiconductor image sense chip (102) after drying up, the transparent layer (140A) being a single layer structure. Glenn et al fail to explicitly disclose that the liquefied gelatinous material form a transparent layer having a thickness equal to a height of each of the conducting wire. Park et al disclose an epoxy compound (50) dispensed over the semiconductor chip (10) with a thickness equal to a height of each of the conducting wires (40). It would have been obvious for one ordinary skill in the art to use an epoxy compound (50) to cover the entire top plane surface of the semiconductor chip (10) as disclosed by Park et al in order to protect the image semiconductor chip (10) from external contamination such as moisture or dust and therefore improving the durability of the chip scale package (100) allowing it to function at an optimal level due to increased signal response relative to sound conducting wire (40) contact between the circuit board and the semiconductor image chip (10), (see figure 10, column 3, lines 55-67, column 4, lines 1-14).

As to claim 2, Glenn et al disclose a chip scale package (100) with a transparent layer (140A) with a top face parallel to the top face (102F) of the semiconductor image sense chip (102) and a periphery (PR) covered by a shelter (130S) to prevent the light from laterally penetrating into the chip scale package structure (100) and influencing the

quality of the image that is collected by the chip scale package structure (100), (see figure 3, column 7, lines 1-5).

As to claim 3, Glenn et al disclose a chip scale package (100) with metal solder ball (122A, 122B) is planted on a free end of each of the conducting wires (118C, 118D) and electrically connected to a flexible printed circuit (FPC), the FPC having a window (110) defined and corresponding to a sensing area (104) of the semiconductor image sense chip (102) and a conducting circuit formed on the bottom face of the FPC, the conducting circuit including multiple first solder points (114) formed near a periphery (PR) of the window (110) and the number of the first solder points (114) corresponding to that of the conducting wire (118C, 118D), the conducting circuit having multiple second solder points (116) formed near one side of the FPC, (see figure 1, column 5, lines 5-13, see figure 3, column 8, lines 1-12).

As to claim 4, Glenn et al disclose a chip scale package (100) with second solder points (116, 116B) arranged in an array, (see figure 1).

As to claim 8, Glen et al disclose a chip scale package (100) with a transparent layer (140A) covering the semiconductor image sense chip (102). Glen et al fail to disclose the transparent layer is made from a gelatinous liquefied material. Park et al disclose an epoxy compound (50) dispensed over the semiconductor chip (10). It would have been obvious for one ordinary skill in the art to use an epoxy compound (50) to cover the entire top plane surface of the semiconductor chip (10) as disclosed by Park et al in order to protect the image semiconductor chip (10) from external contamination such as moisture or dust and therefore improving the durability of the chip scale

package (100) allowing it to function at an optimal level, (see figure 10, column 3, lines 55-67, column 4, lines 1-14).

As to claim 9, Glenn et al disclose a chip scale package (100) with a transparent layer (140A) with a top face parallel to the top face (102F) of the semiconductor image sense chip (102) and a periphery (PR) covered by a shelter (130S) to prevent the light from laterally penetrating into the chip scale package structure (100) and influencing the quality of the image that is collected by the chip scale package structure (100), (see figure 3, column 7, lines 1-5).

As to claim 10, Glenn et al disclose a chip scale package (100) with a metal solder ball (122A, 122B) is planted on a free end of each of the multiple bumps (112A, 112B) and electrically connected to a flexible printed circuit (FPC), the FPC having a window (110) and corresponding to a sensing area (104) of the semiconductor image sense chip (102) and a conducting circuit including multiple first solder points (114) formed near a periphery (PR) of the window (110), the number of the first solder points (114) corresponding to that of the bumps (112A, 112B), the conducting circuit including multiple second solder points (116) formed near one side of the FPC, (see figure 1, column 5, lines 1-5, figure 3, column 7, lines 1-17, column 8, lines 1-11).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Williams whose telephone number is 571-272-8538. The examiner can normally be reached on 8:30a.m. to 5:30a.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephone B. Allen
Primary Examiner